REMARKS

Attached hereto is an excess claims fee letter and fee and a Petition and fee for extension of time.

Claims 1-23 are all the claims presently pending in this application. Claims 19-23 have been added to claim additional features of the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to claim 3. Applicant believes that the claim amendments above address the Examiner's concern and requests that the Examiner reconsider and withdraw this objection.

Claims 1, 2, 8-10, 12-16, and 18 stand rejected under 35 U.S.C. §102(e) as being anticipated by Levy (U.S. Patent No. 5,923,892). Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy and in view of Irwin (U.S. Patent No. 4,695,945). Claims 4-7 and 11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Levy and in view of Schmidt et al. (U.S. Patent No. 5,727,227). Claim 17 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Levy and in view of Yamanaka (U.S. Patent No. 4,774,625).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a microprocessor system for executing instructions described in a program. A main processor executes by hardware instructions which belong to a first instruction set and executes by software instructions which belong to a second instruction set. The main processor includes an interrupt request reception circuit.

A co-processor operative under the control of the main processor autonomously fetches an instruction belonging to the second instruction set to execute the same by its hardware. The co-processor includes an interrupt request generation circuit connected to the interrupt request reception circuit by way of at least one signal line.

An advantage of the encoded interrupt request generation/request circuit, in the combination of the invention, is that the main processor is able to efficiently handle the processing of the instruction by using interrupt vectors.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Levy anticipates the invention of claims 1-2, 8-10, 12-16 and 18, and, when combined with Irwin, renders obvious claim 3. The Examiner further alleges that Levy, when combined with Schmidt, renders obvious claims 4-7 and 11, and, when combined with Yamanaka, renders obvious claim 17. Applicant submits, however, that there are elements of the invention of these claims which are neither taught nor suggested by Levy.

That is, although the Examiner's position is that the embodiment discussed at lines 48-51 of column 9 and lines 8-36 of column 10 of Levy, by reason of omitting some of the instructions to simplify the coprocessor, is similar in some respects to the present invention,

the mechanism in Levy differs.

More specifically, Levy does not use the technique of interrupt vectors. Instead, as clearly described at lines 22-28 of column 10, the main processor in Levy simply retrieves the current operational state of the coprocessor via the expansion bus and, using this retrieved state information, executes the exception instruction.

In contrast, the present invention uses a technique in which the exception instruction is identified to the main processor by information on the signal line(s) between the interrupt request generation circuit in the co-processor and the interrupt request reception circuit. In exemplary embodiments, a plurality of signal lines allows an encoding, thereby providing information that is then converted into an interrupt handler address that points to the instruction set necessary for the main processor to deal with the instruction.

The interrupt vector technique is faster and more efficient than the technique such as used in Levy in which the main processor must identify the instruction and retrieve the appropriate instructions from memory.

Although the Examiner urges a combination of Schmidt with Levy in order to incorporate interrupt vectors into Levy, such combination would not be proper for at least two reasons.

First, Schmidt requires an interrupt co-processor to handle the interrupt vectors. There is no such interrupt co-processor in Levy. Second, and even more important, the technique used in Schmidt would change the principle of operation in Levy. Therefore, Schmidt cannot be combined with Levy under MPEP §2143.01: "The proposed modification cannot change the principle of operation of a reference".

The Irwin and Yamanaka references are introduced for reasons unrelated to this

deficiency in Levy and, therefore, do not overcome this deficiency in Levy.

Hence, turning to the clear language of claim 1, there is no teaching or suggestion in Levy of: "... said main processor having an interrupt request reception circuit; ... said co-processor having an interrupt request generation circuit, said interrupt request generation circuit connected to said interrupt request reception circuit by way of a plurality of signal lines."

Additionally, Applicant traverses the following points in the rejection.

Relative to the motivation to combine references, the Examiner uses the incorrect legal standard "... a person of ordinary skill in the art ... would have recognized...." (Emphasis by Applicant). The correct standard to use is: whether the prior art reference suggests the combination. The standard used by the Examiner is clearly a statement of improper hindsight.

Relative to the urged combination of Yamanaka with Levy, such combination would be improper since the Yamanaka operation processors 17a, 17b, 17c are slave processing units, rather than the autonomous co-processors of Levy.

Relative to claim 4, Schmidt does not teach the technique in which dedicated interrupt vectors are used for more-frequently-executed instructions.

Relative to claim 5, Schmidt does not teach the technique in which multiple instructions are assigned to one interrupt vector.

Relative to claims 6 and , Schmidt does not teach a priority between interrupt vectors, let alone using dedicated interrupt vectors for higher priority interrupts and multiple-instruction interrupt vectors for lessor priority interrupts.

Relative to claim 8, the stack in Levy does not hold data generated in the course of execution, as shown in the present application in Figures 2A and 2B. That is, line 20 of

column 12 clearly indicates that only operands (e.g., not data generated therefrom) are stored in the stack.

Relative to claim 10, Levy does not have a status register that the main processor periodically accesses to check whether the coprocessor has encountered an exception instruction. The closest analogy in Levy is the instruction trap flag described at lines 54-59 of column 9. However, the content of this flag is directly presented to the main processor. The main processor does not "periodical access" a register to determine whether the coprocessor is asking for assistance, as the plain language of the claim requires.

Relative to claim 14, Levy does not have a stack-top register (e.g., see Figures 8A, 8B, and 10 and item 270A of Figure 11 of the present application).

Relative to claim 15, Levy, therefore, also does not have a cache memory provided between the stack memory and the stack-top register (e.g., see item 270C in Figure 11 of the present application). Similarly, Levy inherently fails to describe the definition in claim 16.

III. FORMAL MATTERS AND CONCLUSION

The Examiner also objected to the figures and, more specifically, to Figure 12 by alleging that the text fails to provide a description for the label S290H. In response, Applicant directs the Examiner's attention to line 8 on page 39, wherein is described the purpose of this label. Accordingly, applicant requests that the Examiner reconsider and withdraw this objection.

Finally, Applicant has amended the title to address the Examiner's concern.

In view of the foregoing, Applicant submits that claims 1-23, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the

application is in condition for allowance. The Examiner is respectfully requested to pass the application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Attorney's Deposit Account No. 50-0481.

Respectfully Submitted,

Date: 3/24/04

Frederick E. Cooperrider
Registration No. 36, 769

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254